

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

STEPHEN BOYD, ET AL.

Application No.: 09/752,541

Filed: December 29, 2000

For: **A Parser For Signomial And Geometric Programs**

Art Group: 2124

Examiner: Tuan A. Vu

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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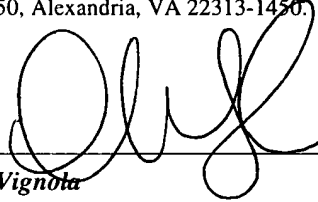
Respectfully submitted,


BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Robert B. O'Rourke, Reg. No. 46,972

12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
Telephone: (408) 720-8300

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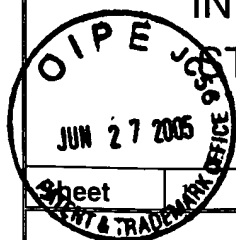

Carla Vignola

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)


 Sheet of 6
Complete if Known

Application Number	09/752,541
Filing Date	12-29-00
First Named Inventor:	Boyd, et al.
Art Unit	2124
Examiner Name	Tuan A. Vu
Attorney Docket Number	004363.P001

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)				
		US-	5,973,524	10/26/1999	Martin	
		US-	6,269,277 B1	07/31/2001	Hershenson	
		US-	4,827,428	05/02/1989	Dunlop, et al.	
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		US-	5,754,826	05/19/1998	Gamal, et al.	
		US-	5,633,807	05/27/1997	Fishburn, et al.	
		US-	5,055,716	10/8/1991	El Gamel	
		US-	5,289,021	02/22/1994	El Gamel	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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		GB	2 131 228 A		6/13/1984	RCA Corporation		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary) JUN 27 2005 U.S. PATENT & TRADEMARK OFFICE		Application Number	09/752,541
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		MEDIERO, F., et al., "A Vertically Integrated Tool For Automated Design Of Sigma Delta Modulators", IEEE Journal of Solid-State Circuits, Vol. 30., No. 7, July 1, 1995, pp. 762-767.	
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NON PATENT LITERATURE DOCUMENTS			
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		HERSHENSON, M., et al., "GPCAD: A Tool for CMOS Op-Amp Synthesis" 8 pages, Proceedings of the IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 296-303, November 1998.	
		HERSHENSON, M., et al., "Posynomial models for MOSFETs" 9 pages, July 7, 1998.	
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		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
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		MAULIK, P., et al., "Sizing of Cell-Level Analog Circuits Using Constrained Optimization Techniques" pp. 233-241, IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993.	
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		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, http://www.siam.org/books/wright , Printed August 19, 1998.	
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		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.	
		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Design.	
		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.	
		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.	

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		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.		
		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.		
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		HUNTER, A., et al., "Combining Advanced Process Technology and Design for Systems Level Integration", IEEE Proceedings, pages 245-250, First International Symposium On Quality Electronic Design, March 20, 2000		